



PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

October 12, 2006

Date

Alex Beggs

Alexandra Beggs

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant	: Nathan R. Brown	Attorney Docket No.:	500200.05
Patent No.	: US 6,852,017 B2	Serial No.	: 09/910,638
Issue Date	: February 8, 2005	Filed	: July 20, 2001
Title	: METHOD AND APPARATUS FOR CHEMICAL-MECHANICAL PLANARIZATION OF MICROELECTRONIC SUBSTRATES WITH A CARRIER AND MEMBRANE		

**REQUEST FOR CERTIFICATE OF CORRECTION**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**Certificate**  
**OCT 18 2006**  
**of Correction**

Sir:

A Certificate of Correction under 35 U.S.C. § 254 is respectfully requested for the above-identified patent in order to correct Patent and Trademark Office errors made during the printing of the patent. The changes in the patent needed to correct the errors are as follows:

<u>Column, Line</u>	<u>Reads</u>	<u>Should Read</u>
Item (56), U.S. Patent Documents	[Omitted references]	--6,290,572 B1 9/2001 Hofmann.....451/5 5,769,699 6/1998 Yu.....451/528 6,135,858 10/2000 Takahashi.....451/41--
Column 3, Line 57	"the thicket portion"	--the thicker portion--
Column 8, Line 66	[Omitted	--5. A method for removing material from a

**OCT 18 2006**

- claims] microelectronic substrate, comprising:
- providing a substrate holder that carries the microelectronic substrate and at least one membrane having a first membrane portion and a second membrane portion, the at least one membrane disposed between the substrate holder and the microelectronic substrate;
  - engaging the microelectronic substrate with a planarizing medium;
  - moving at least one of a first part of the microelectronic substrate and the planarizing medium relative to the other at a first rate;
  - moving at least one of a second part of the microelectronic substrate and the planarizing medium relative to the other at a second rate less than the first rate; and
  - removing material from the first and second parts of the microelectronic substrate at approximately equal rates by biasing the first part of the microelectronic substrate against the planarizing medium with the first membrane portion having a first thickness and biasing the second part of the microelectronic substrate against the planarizing medium with the second membrane portion having a second thickness greater than the first thickness.
6. The method of claim 5 wherein engaging the microelectronic substrate with the planarizing medium includes engaging the microelectronic substrate with a polishing pad.
7. The method of claim 5 wherein moving at least one of the first part of the microelectronic substrate and the planarizing medium includes moving at least one of a first annular part of the microelectronic substrate and the planarizing medium, further wherein moving at least one of the second part of the

microelectronic substrate and the planarizing medium includes moving at least one of the planarizing medium and a second annular part of the microelectronic substrate positioned radially inwardly from the first annular part of the microelectronic substrate.

8. The method of claim 5 wherein the at least one membrane has a first surface facing toward the microelectronic substrate and a second surface facing generally opposite the first surface, further wherein biasing the microelectronic substrate against the planarizing medium includes biasing a generally flat support member against the second surface of the membrane.

9. The method of claim 5 wherein biasing the microelectronic substrate against a planarizing medium includes biasing the microelectronic substrate against a first portion of a polishing pad, further wherein moving at least one of the microelectronic substrate and the planarizing medium includes advancing the polishing pad from a supply roller to a take-up roller to engage a second portion of the polishing pad with the first and second parts of the microelectronic substrate.--

The above errors for which correction is requested under 35 U.S.C. § 254 were made in the printing of the patent . The errors are considered sufficiently important to justify the processing of a Certificate of Correction under 35 U.S.C. § 254. A Form PTO-1050, in duplicate, is enclosed herewith.

Favorable consideration of this Request is respectfully requested.

Respectfully submitted,

Date: Oct. 10, 2006

By: Edward W. Bulchis

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Enclosures:

Postcard

Form PTO-1050 (+ copy)

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OCT 18 2006

**UNITED STATES PATENT AND TRADEMARK OFFICE  
CERTIFICATE OF CORRECTION**

PATENT NO. : US 6,852,017 B2  
DATED : February 8, 2005  
INVENTOR(S) : Nathan R. Brown

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Column 3, Line 57	"the thicket portion"	--the thicker portion--
Column 8, Line 66	[Omitted claims]	--5. A method for removing material from a microelectronic substrate, comprising: providing a substrate holder that carries the microelectronic substrate and at least one membrane having a first membrane portion and a second membrane portion, the at least one membrane disposed between the substrate holder and the microelectronic substrate; engaging the microelectronic substrate with a planarizing medium; moving at least one of a first part of the microelectronic substrate and the planarizing medium relative to the other at a first rate; moving at least one of a second part of the microelectronic substrate and the planarizing medium relative to the other at a second rate less than the first rate; and removing material from the first and second parts of the microelectronic

OCT 18 2005

substrate at approximately equal rates by biasing the first part of the microelectronic substrate against the planarizing medium with the first membrane portion having a first thickness and biasing the second part of the microelectronic substrate against the planarizing medium with the second membrane portion having a second thickness greater than the first thickness.

6. The method of claim 5 wherein engaging the microelectronic substrate with the planarizing medium includes engaging the microelectronic substrate with a polishing pad.

7. The method of claim 5 wherein moving at least one of the first part of the microelectronic substrate and the planarizing medium includes moving at least one of a first annular part of the microelectronic substrate and the planarizing medium, further wherein moving at least one of the second part of the microelectronic substrate and the planarizing medium includes moving at least one of the planarizing medium and a second annular part of the microelectronic substrate positioned radially inwardly from the first annular part of the microelectronic substrate.

8. The method of claim 5 wherein the at least one membrane has a first surface facing toward the microelectronic substrate and a second surface facing generally opposite the first surface, further wherein biasing the microelectronic substrate against the planarizing medium includes biasing a generally flat support member against the second surface of the membrane.

9. The method of claim 5 wherein biasing

OCT 18 2006

the microelectronic substrate against a planarizing medium includes biasing the microelectronic substrate against a first portion of a polishing pad, further wherein moving at least one of the microelectronic substrate and the planarizing medium includes advancing the polishing pad from a supply roller to a take-up roller to engage a second portion of the polishing pad with the first and second parts of the microelectronic substrate.--

MAILING ADDRESS OF SENDER:

**DORSEY & WHITNEY LLP**  
**1420 Fifth Avenue, Suite 3400**  
**Seattle, Washington 98101**

Patent No. US 6,852,017 B2

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FORM PTO-1050 (REV. 3-82)

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OCT 18 2006

# UNITED STATES PATENT AND TRADEMARK OFFICE

## CERTIFICATE OF CORRECTION

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OCT 18 2006



substrate at approximately equal rates by biasing the first part of the microelectronic substrate against the planarizing medium with the first membrane portion having a first thickness and biasing the second part of the microelectronic substrate against the planarizing medium with the second membrane portion having a second thickness greater than the first thickness.

6. The method of claim 5 wherein engaging the microelectronic substrate with the planarizing medium includes engaging the microelectronic substrate with a polishing pad.

7. The method of claim 5 wherein moving at least one of the first part of the microelectronic substrate and the planarizing medium includes moving at least one of a first annular part of the microelectronic substrate and the planarizing medium, further wherein moving at least one of the second part of the microelectronic substrate and the planarizing medium includes moving at least one of the planarizing medium and a second annular part of the microelectronic substrate positioned radially inwardly from the first annular part of the microelectronic substrate.

8. The method of claim 5 wherein the at least one membrane has a first surface facing toward the microelectronic substrate and a second surface facing generally opposite the first surface, further wherein biasing the microelectronic substrate against the planarizing medium includes biasing a generally flat support member against the second surface of the membrane.

9. The method of claim 5 wherein biasing

OCT 18 2006

the microelectronic substrate against a planarizing medium includes biasing the microelectronic substrate against a first portion of a polishing pad, further wherein moving at least one of the microelectronic substrate and the planarizing medium includes advancing the polishing pad from a supply roller to a take-up roller to engage a second portion of the polishing pad with the first and second parts of the microelectronic substrate.--

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**1420 Fifth Avenue, Suite 3400**  
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Sheet 1 of 1

FORM PTO-1449  
(REV. 7-00)

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO.  
500200.05

APPLICATION NO.  
09/910,638

**INFORMATION DISCLOSURE STATEMENT**  
(Use several sheets if necessary)

APPLICANT(S)  
Nathan R. Brown

FILING DATE  
July 20, 2001

GROUP ART UNIT  
3729

**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
AB	AA	5,769,699	06/23/98	Yu	451	528	
AB	AB	6,290,572 B1	09/18/01	Hofmann	451	5	
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						

**FOREIGN PATENT DOCUMENTS**

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	AK							
	AL							
	AM							
	AN							
	AO							

**OTHER PRIOR ART** (Including Author, Title, Date, Pertinent Pages, Etc.)

	AP	
	AQ	
	AR	

EXAMINER

*Alvin J. Grant*

DATE CONSIDERED

11/15/04

OCT 18 2006

\* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

Form PT-27/1/194

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Sheet 1 of 1

FORM PTO-1449 (REV.7-10)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 500200.05	APPLICATION NO. 09/910,638
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT(S) Nathan R. Brown	
		FILING DATE July 20, 2001	GROUP ART UNIT 3729

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
AK	AQ	5,730,642	3/24/98	Sandhu et al.	451	6	
AK	AP	5,733,182	3/31/98	Muramatsu et al.	451	289	
AK	AO	5,766,058	6/16/98	Lee et al.	451	41	
AK	AN	5,769,692	6/23/98	Pasch et al.	451	41	
AK	AM	5,769,696	6/23/98	Lee et al.	451	287	
AK	AL	5,791,973	8/11/98	Nishio	451	41	
AK	AK	5,888,120	3/30/99	Doran	451	41	
AK	AJ	5,964,646	10/12/99	Kassir et al.	451	41	
AK	AI	5,997,385	12/7/99	Nishio	451	56	
AK	AH	6,019,868	2/1/00	Kimura et al.	156	345	
AK	AG	6,027,401	2/22/00	Saito et al.	451	398	
AK	AF	6,036,587	3/14/00	Tolles et al.	451	288	
AK	AE	6,050,882	4/18/00	Chen	451	41	
AK	AD	6,074,289	6/13/00	Murakami et al.	451	388	
AK	AC	6,083,090	7/4/00	Bamba	451	288	
AK	AB	6,093,085	7/25/00	Yellitz et al.	451	41	
AK	AA	6,135,858	10/24/00	Takahashi	451	41	

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
AR	2,173,639	10/11/96	Canada				

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

AS							
AT							

EXAMINER <i>Alvin D. Grant</i>	DATE CONSIDERED 11/15/04	OCT 18 2005
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